Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.013”**



**ANODE**

**.0055 x .0055”**

**.013”**

**Top Material: Al**

**Backside Material: Au As**

**Bond Pad Size: .0055”**

**Backside Potential: CAHTHODE**

**Mask Ref: CPZ28X**

**APPROVED BY: DK DIE SIZE .013” X .013” DATE: 3/17/22**

**MFG: CENTRAL SEMI THICKNESS .006” P/N: 1N5530B**

**DG 10.1.2**

#### Rev B, 7/1